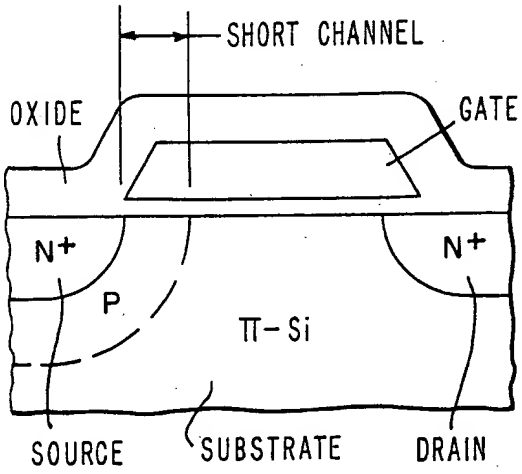
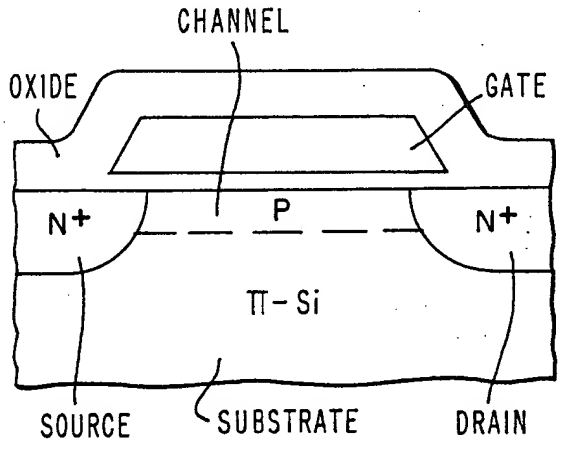
DMOS FET WITH COMMON FIELD AND CHANNEL DOPING

B. L. Crowder and V. L. Rideout



DMOS FET

FIG. 1A



NMOS FET

FIG. 1B

This article describes how the short channel doping and the field doping may be combined to reduce processing steps in a DMOS FET (double-diffused metal-oxide-silicon field-effect transistor). A drain side blocking mask, rather than a source side window opening, is used for the common channel/field boron implantation. Due to the asymmetrical channel doping, the DMOS FET offers improved performance over a conventional NMOS FET (n-channel MOS FET) having the same source-to-drain spacing. These two devices are shown in Figs. 1A and 1B. Compared to an NMOS device, a DMOS device requires an additional masking step to provide the p-type doping for the short channel (injection region) on the source side of the device. An additional diffusion step is also required. Described here is a novel means for fabricating DMOS devices in which the p-type short channel doping under the gate oxide and the p-type field doping under the field isolation oxide are provided in the same step, thereby simplifying the process.

Two processing approaches are described. In the first one, the gate pattern is defined before the field pattern. Then a self-registering contact [*] can be used over the gate. This is not required but is advantageous because the polysilicon layer cannot be used for interconnections. Processing simplicity is the primary attraction of this approach.

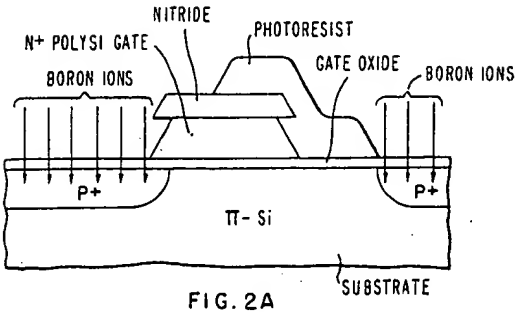


FIG. 2A

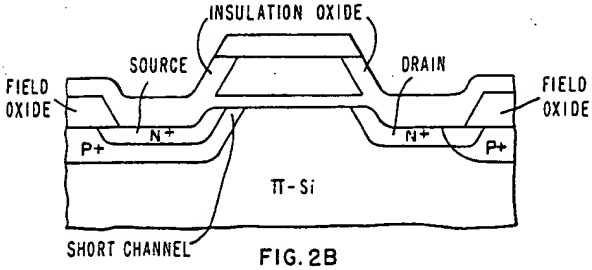


FIG. 2B

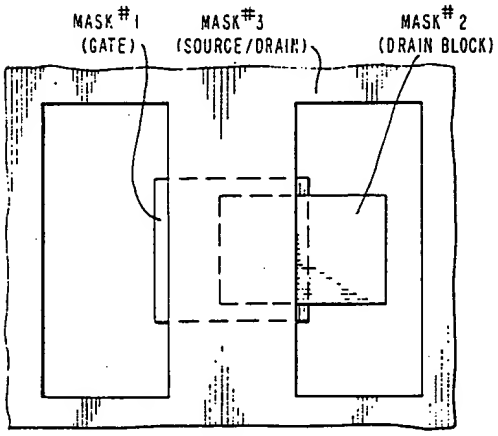


FIG. 2C

A second and slightly more complicated approach is described which facilitates the fabrication of depletion-mode devices. Here the field pattern precedes the gate pattern. The initial field oxide thickness must be small enough so that the boron implantation can penetrate through to the field region. Again, a self-registering gate contact can be employed, if desired.

Fig. 2 shows side and top views of the DMOS structure fabricated using the simpler common channel/field process. The first step of the process is to grow the gate oxide of 500 Å thickness over the entire wafer. Then a CVD (chemical vapor deposition) polysilicon layer is deposited, doped n+, and an oxidation barrier layer (silicon nitride) is

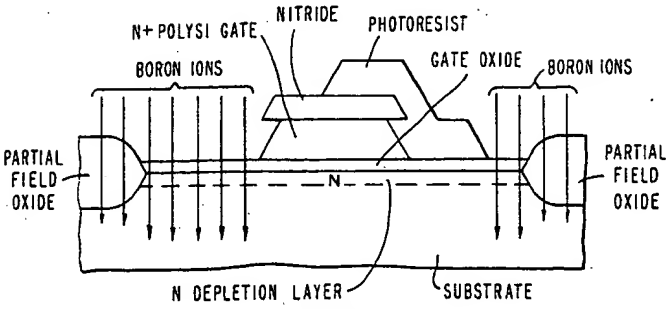


FIG. 3A

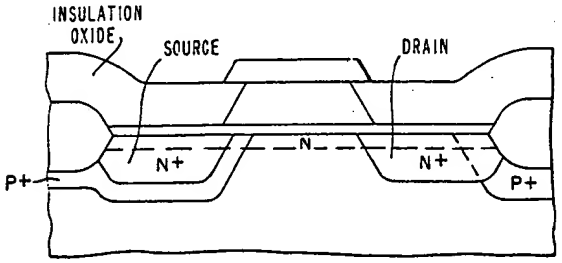


FIG. 3B

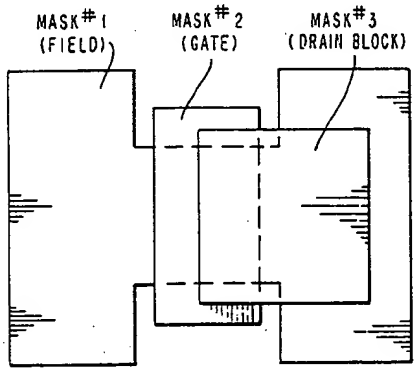


FIG. 3C

deposited over the polysilicon. Thin oxide layers may be used on either side of the nitride layer to aid in its delineation and removal. Now one etches down through the oxidation barrier and polysilicon to define the gate pattern.

The next step is to define a resist region to block p-type channel/field doping on the drain side of the device (Fig. 2A). This is in contrast to other DMOS fabrication procedures in which an opening is commonly provided on the source side to obtain the DMOS channel doping. With the new approach the p-type doping will occur everywhere except on the drain side of the device and directly under the polysilicon gate. The polysilicon is typically 3500 Å thick and the nitride layer 500 Å

thick. Now the drain-side resist block is removed by dissolving. Next, the field isolation oxide is grown about 3000 Å thick. This need not be the final field oxide thickness as it will be increased later by the growth of the insulation oxide over the subsequently formed source/drain regions. The field oxide must only be thick enough so that the source/drain implant does not penetrate through it.

The next masking step (#3) is used to open the device regions by etching. The source/drain implant is performed and a thick insulation oxide of 3000 Å or more is grown over the entire structure except for the gate which is still protected by the nitride layer (Fig. 2B). Now the nitride layer is removed by dissolving.

Mask 4 (not shown) is used to open contact holes to the source and drain regions. As the insulation oxide is not greatly different in thickness from the field oxide thickness, holes to the substrate can also be opened in this step. Then the metal pattern (mask 5, not shown) is delineated.

Some unique features of this approach are:

1. The field and DMOS short channel doping are performed at the same time.

2. The field oxidation also serves to drive in the DMOS short channel doping.

3. The insulation oxide growth also thickens the field oxide.

4. The gate pattern is self-aligned to the field isolation at the edges of the gate. This yields a very small area device.

The simple DMOS process described above has several shortcomings that can be alleviated with a somewhat more complex structure. The first shortcoming is that it is difficult, but not impossible, to incorporate a depletion-mode n-type doping region under the gate. One way to incorporate this into the simple process is to blanket implant the wafer with an n-type shallow doping after growing the gate oxide, then define the polysilicon and the drain block patterns, and finally implant the field p-type implant which must overcompensate the n-type doping in the field region. However, if the n-type depletion-mode doping is desired only in the device regions and not in the field regions, a different approach must be used; the device pattern must be defined before the gate pattern. Another shortcoming is that the entire field growth is performed after the field implant. Thus, the boron field doping experiences the maximum possible depletion. We will presently describe p-type implantation through a thicker partially-grown field oxide. Finally, the polysilicon lines can only be used as gates. This restriction strongly suggests using a self-registered gate contact [*].

Fig. 3 illustrates the thin field procedure. One begins by growing

a partial field oxide of 1500-3000 Å thickness (about 2500 Å being preferable). Then, using first the field pattern, one removes the partial field oxide in the device areas. Next, after growing the 500 Å gate oxide, the shallow n-type depletion-mode implant is made in the device areas. Then the polysilicon layer is deposited, doped n+, and the oxidation barrier layer (silicon nitride) is deposited. Again, oxide layers may be provided on either side of the nitride layer to aid in its delineation and removal. Then the gate pattern (mask #2) is defined by etching. Now the field implant is performed. The boron energy must be high enough so that the implant penetrates the field oxide (e.g., 100 KeV at $1x10^{12}$ cm^{-2}). The drain block (mask #3) is in place during the boron implantation (Fig. 3A).

After removing the drain block, the n+ source/drain implant is performed. Now the energy must be low enough so that the field oxide is not penetrated (e.g., As^{75} at 100 KeV, $4x10^{15}$ cm^{-2}). Then the insulation oxide is grown over the source/drain and field but not over the gate which is still protected by the nitride layer (Fig. 3B). Finally, the nitride is removed by dissolving, contact holes are opened to the source and drain (mask #4, not shown), and the metal pattern is delineated (mask #5, not shown).

The second approach offers the difficulty that the field doping occurs quite deep in the source and drain regions, and, therefore, a p+ layer may occur beneath the n+ doping, thereby raising the depletion capacitance of the n+ lines. Nevertheless, a depletion-mode device is provided with an n-type doping which does not overlay the p-type field doping.

Reference

[*] V. L. Rideout, "Masking for One-Device Cell Memories Using Self-Registering Metal-to-Polysilicon Contacts," IBM Technical Disclosure Bulletin 17, 2802 (February 1975).